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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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GROUP 2800

Application Number: 10/605,699
Filing Date: October 21, 2003
Appellant(s): CHATTY ET AL.

Myron Keith Wyche
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 07/03/06 appealing from the Office action mailed 11/29/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,675,170	KIM	10-1997
4,642,667	MAGEE	2-1987

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-10 and 15-31 are rejected under 35 U. S. C. 102(b) as being anticipated by Kim et al. (US Pat. 5,675,170).

Regarding claims 1 and 22, Kim discloses, in figs. 3 and 4, a method of forming a CMOS semiconductor structure having improved latch-up robustness, the method comprising the steps of: providing a substrate 1 including an injection site (I/O) and a plurality of a CMOS circuit structures (NMOS/PMOS), wherein at least one of circuit structures has a susceptibility to a latch-up condition (col. 3, lines 8-16); and forming a plurality of contact regions (22/23/41/32/33/2/3/4) inter-spaced a varying distance between circuit structures.

Regarding claims 2, 3, 23 and 24, Kim discloses the distance varies with the proximity of contact regions to injection site; wherein distance varies with the susceptibility of circuit structures to a latch-up condition (figs. 3-4 and col. 3, lines 8-16).

Regarding claims 4-6 and 25-27, Kim discloses the plurality of contact regions comprises a first contact region 22 and a second contact region 23 spaced a first distance apart, and second contact region 23 and a third contact region 41 spaced a second distance apart different from first distance (figs. 3-4).

Regarding claim 7, Kim discloses the substrate comprises a well region having formed therein latch-up susceptible circuit structure (figs. 3-4).

Regarding claim 8, Kim discloses the well region (3/4) is n-type (figs. 3-4).

Regarding claim 9, Kim discloses the n-type well region (3/4) includes at least one contact comprising an n+ region (41/34) (figs. 3-4).

Regarding claim 10, Kim discloses at least one contact is coupled to Vdd (figs. 3-4).

Regarding claim 15, Kim discloses the plurality of contact regions are located along an axis and arranged vertically relative to axis (fig. 3).

Regarding claim 16, Kim discloses the plurality of contact regions are located along an axis and arranged horizontally relative to axis (fig. 3).

Regarding claim 17, Kim discloses the plurality of contact regions are located along an axis and arranged concentrically relative to axis (fig. 3).

Regarding claims 20 and 30, Kim discloses the distance increases as the distance of plurality of contact regions from injection site increases (figs. 3 and 4).

Regarding claims 21 and 31, Kim discloses the plurality of contact regions are located along an axis so that spacing between adjacent contact regions increases as the distance from injection site increases (figs. 3 and 4).

Regarding claims 18, 19, 28 and 29, the limitations " wherein said distance is determined such that ...." (claims 18 and 28) or " wherein said external current injector is a cable discharge ...." (claims 19 and 29) are merely functional/intended use limitations that do not structurally distinguish the claimed invention over the prior. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and In re Otto, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963).

2. Claims 1, 7 and 11-14 are rejected under 35 U. S. C. 102(b) as being anticipated by Magee (US Pat. 4,642,667).

Regarding claim 1, Magee discloses, in figs. 1 and 2, a method of forming a semiconductor structure having improved latch-up robustness, the method comprising the steps of: providing a substrate 11 including an injection site (I/O) and a plurality of circuit structures (CMOS), wherein at least one of circuit structures has a susceptibility to a latch-up condition (col. 1, line 62 through col. 2, line 53); and forming a plurality of contact regions (32/33/34/35/36) inter-spaced a varying distance between circuit structures.

Regarding claims 7 and 11, Magee discloses, in figs. 1 and 2, substrate comprises a p-well region having formed therein latch-up susceptible circuit structure.

Regarding claim 12, Magee discloses, in figs. 1 and 2, a p-type well region includes at least one contact comprising a p+ region.

Regarding claim 13, Magee discloses, in figs. 1 and 2, at least one contact is coupled to ground.

Regarding claim 14, Magee discloses, in figs. 1 and 2, at least one contact is coupled to Vss.

(10) Response to Argument

A. <u>The rejection of claims 1-10 and 15-31 under 35 U. S. C. 102(b) as being anticipated by Kim et al. (US Pat. 5,675,170).</u>

Appellant's arguments have been fully considered but they are not persuasive. Appellant begin by arguing that Kim reference does not teaches an injection site associated with CMOS semiconductor structure that is compatible with modern CMOS technologies. As in all semiconductor devices, the injection site (data I/O pad) is a part of a CMOS (PMOS/NMOS) structure. The CMOS structure is clearly taught by Kim (col. 2, lines 34-42) that "*a NMOS transistor* having one terminal which is connected to a grounded voltage source Vss and the other terminal which *is connected to a data input and output pad*; *a PMOS transistor* having one terminal which is connected to a bias voltage source Vcc and the other terminal which *is connected to the data input and output pad*" *emphasis by examiner.* Kim could not teach more clearly the modern CMOS structure to Applicant's arguments (page. 6). However, the difference is not sufficient to negate the CMOS structure of Kim with Applicant's device. As mentioned in the above rejection, Kim discloses, in figs. 3 and 4, a CMOS semiconductor structure having a substrate 1 including an injection site (I/O) and a plurality of a CMOS circuit structures

(NMOS/PMOS), wherein at least one of circuit structures has a susceptibility to a latch-up condition (col. 3, lines 8-16); and forming a plurality of contact regions (22/23/41/32/33/2/3/4) inter-spaced a varying distance between circuit structures.

Appellant's arguments that the claimed invention is directed toward a modern CMOS semiconductor structure. First, nowhere in the specification is defined a specific structure of a modern CMOS. Both Kim's CMOS structure and Applicant's "modern" CMOS are CMOS devices concerned with the interruption of the movement of minority carriers so that the generation of a latch-up is prevented (i.e. Kim and the presently claimed invention are both CMOS structure and have the same functionality). Second, the term "modern CMOS" is not well-known in the art and does not distinguish over the structure of Kim because the language "modern" is merely a label and the meaning "modern" is indefinite as to scope. Finally, whether the device is a modern CMOS structure or conventional CMOS structure, the injection site should be able to associate with the CMOS structure. This is not dependent on the type of CMOS structure being used.

Applicant's argue that "in the claimed invention and in more modern CMOS technologies the area under I/O pads is not available because additional circuits are placed under the I/O pads due to restrains on integrated circuit area and requirements for increased integrated circuit functionality. However, Applicant's arguments are not commensurate with what is claimed, and also appears to be a mere allegation that would not always be required.

On the bottom of page 8, the gist of Appellant's arguments against the anticipatory rejection is primarily based on the functional/operating differences between the CMOS structure of Kim and that of the instant invention such as the structure disclosed by Kim of expanding the

N-well guard ring to collect injected minority carriers to reduce latch-up is not applicable for non-standard latch-up tests "arising from a cable discharge event," (as recited in claims 19 and 29) because it "would require unreasonably large N-well guard ring" which would be "very difficult" to implement in modern CMOS. However, this is not an issue with respect to the claimed invention. This is, because the invention, as set forth in the claims, is clearly directed to an apparatus. No where do the limitations of the claims define the process in which the instant invention is to be operated. Thus, such arguments clearly fail to distinguish the claimed invention from the disclosure of Kim. Moreover, Applicant appears to be merely stating opinion (i.e. "would require", "would be very difficult").

B. The rejection of claims 1-10 and 15-31 under 35 U. S. C. 102(b) as being anticipated by Magee (US Pat. 4,642,667)

Appellant's arguments have been fully considered but they are not persuasive. Appellant argues that the Magee reference does not teach an injection site associated with CMOS semiconductor structure that is compatible with modern CMOS technologies. As discussed above, Magee discloses, in figs. 1 and 2, a semiconductor structure having a substrate 11 including an injection site (I/O) and a plurality of circuit structures (CMOS), wherein at least one of circuit structures has a susceptibility to a latch-up condition (col. 1, line 62 through col. 2, line 53); and a plurality of contact regions (32/33/34/35/36) inter-spaced a varying distance between circuit structures.

The appellant further states in the first paragraph of page 10 that different device (CMOS vs. modern CMOS) produces different results (i.e. structure of Magee is not applicable to

modern CMOS semiconductor structures that have restraints on integrated circuit area…..). However, these results do not deter from the fact that structures of the applicant's claimed invention and Magee's disclosed invention are identical. They are both CMOS and even operate identically as transistors wherein a voltage is applied to a gate in between a pair of source/drain regions to induce a current. Therefore, with a claimed structurally and operationally identical to Kim's device, it is undisputable that Magee's invention reads on the claimed invention. Furthermore, as already stated above, the applicant's claimed invention is directed towards apparatus and only those limitations that pertain to the final product structure will be considered. Therefore, for these reasons, the argument of the operating CMOS vs. modern CMOS is not persuasive.

In response to applicant's argument that Magee was not directed toward the problem of reducing latch-up in modern CMOS technologies or in the "CMOS semiconductor structure", the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Applicant's argument however, reads too much into the language "modern CMOS semiconductor structure". Specifically, Applicant's argument requires that the limitation "CMOS device" include not only the structural of the CMOS device already included in claim 1, but also a structural drawn to an arrangement of n+ and p+ taps in Magee is not feasible in a modern CMOS semiconductor structure, which is not recited in claim 1. Rather, the claim simply recites that the "CMOS semiconductor structure" is included "an injection site" which is capable to

protect the CMOS device from "a latch-up condition". Such structure is taught by Magee as discussed and made clear in the above rejection.

Finally, with regard to Applicants objection to the age of the prior art references, contentions that the reference patents are old are not impressive absent a showing that the art tried and failed to solve the same problem notwithstanding its presumed knowledge of the references. See *In re Wright*, 569 F.2d 1124, 193 USPQ 332 (CCPA 1977).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

DAVID VU
PRIMARY EXAMINER

November 22, 2006

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